What Is Claimed Is:

1   1.   An apparatus that facilitates implementing a memory mechanism

2   within an asynchronous switch fabric, comprising:

3   a memory device, wherein the memory device has other than first-in, first-

4   out semantics including one of a random access memory and a stack;

5   a data destination horn, for routing data from a trunk line to a plurality of

6   destinations, wherein the memory device is a destination of the plurality of

7   destinations; and

8   a data source funnel, for routing data from a plurality of sources into the

9   trunk line, wherein the memory device is a source of the plurality of sources.

1   2.   The apparatus of claim 1, further comprising:

2   an asynchronous control structure coupled to the data destination horn,

3   that is configured to control propagation of data through the data destination horn;

4   wherein the asynchronous control structure is additionally coupled to the

5   data source funnel, and is additionally configured to control propagation of data

6   through the data source funnel;

7   wherein the asynchronous control structure uses a destination address

8   associated with the data destination horn for the memory device to control

9   propagation of data to the memory device; and

10   wherein the asynchronous control structure uses the destination address for

11   the memory device to control propagation of data from the memory device.

1   3.   The apparatus of claim 2, wherein a read address for the memory

2   device is shared as a write address of the data destination horn for the memory

3   device, so that an order of memory operations for the memory device is identical

4   to an instruction order for the memory device.

1   4.   The apparatus of claim 3, wherein a literal value associated with an

2   instruction for the memory device can specify one of a write operation and a read

3   operation.

1   5.   The apparatus of claim 4, further comprising a first-in, first-out

2   storage structure interposed between the memory device and the data source

3   funnel so that data delivered from the memory device during the read operation

4   will be available to the data source funnel in a same order as delivered from the

5   memory device.

1   6.   The apparatus of claim 1, further comprising:

2   an asynchronous control structure coupled to the data destination horn,

3   that is configured to control propagation of data through the data destination horn;

4   wherein the asynchronous control structure is additionally coupled to the

5   data source funnel, and is additionally configured to control propagation of data

6   through the data source funnel;

7   wherein the asynchronous control structure uses a source address

8   associated with the data source funnel for the memory device to control

9   propagation of data to the memory device; and

10   wherein the asynchronous control structure uses the source address for the

11   memory device to control propagation of data from the memory device.

1   7.   The apparatus of claim 6, wherein a write address for the memory

2   device is shared as a read address of the data source funnel for the memory device,

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1 so that an order of memory operations for the memory device is identical to an

2 instruction order for the memory device.

1 8. The apparatus of claim 7, wherein a literal value associated with an

2 instruction for the memory device can specify one of a write operation and a read

3 operation.

1 9. The apparatus of claim 8, further comprising a first-in, first-out

2 storage structure interposed between the data destination horn and the memory

3 device so that data delivered from the data destination horn during the write

4 operation will be available to the memory device in a same order as delivered

5 from the data destination horn.

1 10. The apparatus of claim 1, wherein the apparatus converts the

2 memory device with other than first-in, first-out semantics to into a dual-port

3 device with first-in, first-out semantics, wherein read/write order hazards are

4 avoided by assigning read and write control to a single port of the dual-port

5 device.

1 11. A computing system that facilitates implementing a memory

2 mechanism within an asynchronous switch fabric, comprising:

3 a memory device, wherein the memory device has other than first-in, first-

4 out semantics including one of a random access memory and a stack;

5 a data destination horn, for routing data from a trunk line to a plurality of

6 destinations, wherein the memory device is a destination of the plurality of

7 destinations; and

8   a data source funnel, for routing data from a plurality of sources into the

9   trunk line, wherein the memory device is a source of the plurality of sources.

1   12.   The computing system of claim 11, further comprising:

2   an asynchronous control structure coupled to the data destination horn,

3   that is configured to control propagation of data through the data destination horn;

4   wherein the asynchronous control structure is additionally coupled to the

5   data source funnel, and is additionally configured to control propagation of data

6   through the data source funnel;

7   wherein the asynchronous control structure uses a destination address

8   associated with the data destination horn for the memory device to control

9   propagation of data to the memory device; and

10   wherein the asynchronous control structure uses the destination address for

11 the memory device to control propagation of data from the memory device.

1   13.   The computing system of claim 12, wherein a read address for the

2   memory device is shared as a write address of the data destination horn for the

3   memory device, so that an order of memory operations for the memory device is

4   identical to an instruction order for the memory device.

1   14.   The computing system of claim 13, wherein a literal value

2   associated with an instruction for the memory device can specify one of a write

3   operation and a read operation.

1   15.   The computing system of claim 14, further comprising a first-in,

2   first-out storage structure interposed between the memory device and the data

3   source funnel so that data delivered from the memory device during the read

1 operation will be available to the data source funnel in a same order as delivered

2 from the memory device.

1 16. The computing system of claim 11, further comprising:

2 an asynchronous control structure coupled to the data destination horn,

3 that is configured to control propagation of data through the data destination horn;

4 wherein the asynchronous control structure is additionally coupled to the

5 data source funnel, and is additionally configured to control propagation of data

6 through the data source funnel;

7 wherein the asynchronous control structure uses a source address

8 associated with the data source funnel for the memory device to control

9 propagation of data to the memory device; and

10 wherein the asynchronous control structure uses the source address for the

11 memory device to control propagation of data from the memory device.

1 17. The computing system of claim 16, wherein a write address for the

2 memory device is shared as a read address of the data source funnel for the

3 memory device, so that an order of memory operations for the memory device is

4 identical to an instruction order for the memory device.

1 18. The computing system of claim 17, wherein a literal value

2 associated with an instruction for the memory device can specify one of a write

3 operation and a read operation.

1 19. The computing system of claim 18, further comprising a first-in,

2 first-out storage structure interposed between the data destination horn and the

3 memory device so that data delivered from the data destination horn during the

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4   write operation will be available to the memory device in a same order as

5   delivered from the data destination horn.

1   20.   The apparatus of claim 11, wherein the apparatus converts the

2   memory device with other than first-in, first-out semantics to into a dual-port

3   device with first-in, first-out semantics, wherein read/write order hazards are

4   avoided by assigning read and write control to a single port of the dual-port

5   device.

1   21.   A method for implementing a memory mechanism within an

2   asynchronous switch fabric, wherein the memory mechanism is a memory device

3   with other than first-in, first-out semantics including one of a random access

4   memory and a stack, comprising:

5   accepting data from a trunk line to a data destination horn;

6   routing data to a plurality of destinations from the data destination horn,

7   wherein the memory device is a destination of the plurality of destinations;

8   addressing the memory device using a destination address within an

9   asynchronous control structure, wherein the destination address is used to store

10 data in the memory device and to recover data from the memory device;

11   decoding an additional address bit to select one of a memory read and a

12 memory write;

13   providing data to a first-in, first-out storage structure from the memory

14 device;

15   receiving data from the first-in, first-out storage structure at a data source

16 funnel; and

17   applying data from the data source funnel to the trunk line.

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1   22.   A method for implementing a memory mechanism within an

2   asynchronous switch fabric, wherein the memory mechanism includes a memory

3   device with other than first-in, first-out semantics, comprising:

4   accepting data from a trunk line to a data destination horn;

5   routing data to a plurality of destinations from the data destination horn,

6   wherein a first-in, first-out storage structure is a destination of the plurality of

7   destinations;

8   providing data to the memory device from the first-in, first-out storage

9   structure;

10   addressing the memory device using a source address within an

11   asynchronous control structure, wherein the source address is used to store data in

12   the memory device and to recover data from the memory device;

13   decoding an additional address bit to select one of a memory read and a

14   memory write;

15   receiving data from the memory device at a data source funnel; and

16   applying data from the data source funnel to the trunk line.